ATTORNEY DOCKET NO. JESSEN 7-1-4 (JESSEN 12-4-6) **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Isiah O. Oladeji, et al.

Serial No.: 10/699,975

Filed: November 2, 2003

For: MASK LAYER AND INTERCONNECT STRUCTURE FOR DAMASCENE SEMICONDUCTOR MANUFACTURING

Grp./A.U.: 2822

Examiner: Maria F. Guerrero

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ATTENTION: Board of Patent Appeals and Interferences

Sirs:

AMENDED APPEAL BRIEF UNDER 37 C.F.R. §41.37(d)

This amended brief is submitted in furtherance of the Notice of Appeal filed in this application on December 14, 2005; and further in response to the Notification of Non-Compliant Appeal Brief mailed on April 20, 2006. To Appellants' knowledge, no fee is required with the re-filing of this Brief in response to the Notice of Non-Compliance. However, if any fees are required,

the Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 08-2395.

This Brief contains these items under the following headings, and in the order set forth below in accordance with 37 C.F.R. §41.37(c)(1):

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I. REAL PARTY IN INTEREST

The real party in interest in this Appeal is the assignee of the present application, Agere Systems, Inc., a corporation of the State of Delaware.

II. RELATED APPEALS AND INTERFERENCES

No other appeals or interferences will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF THE CLAIMS

Claims 1-5 are cancelled and no claims have been withdrawn. Claims 6-24 are pending in this application, none of which have been allowed. Claims 6-24 and have been rejected under 35 U.S.C. § 103(a), and each of these pending claims are being appealed.

IV. STATUS OF THE AMENDMENTS

No amendments have been filed subsequent to the final rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to methods of fabricating semiconductor devices and relates particularly to formation of dual damascene interconnect structures with low-k dielectric materials, which are typically polymer-based. It is well-known that undesirable reactions occur among these dielectric materials, the associated photoresist materials and the chemical cleaning processes through which the photoresist is removed. Conventionally, a barrier layer film is formed over the low-k dielectric to isolate the low- k dielectric material from the photoresist and related processing.

Independent Claim 1 is directed to a method of forming a dual damascene interconnect structure of an integrated circuit device. The interconnect structure has a low-k dielectric material deposited over an underlying metal layer and comprising the steps of forming a tri-part mask layer overlaying the low-k dielectric material. The mask layer includes a passivation mask film located over the low-k dielectric material, a non-metallic barrier mask film overlaying the passivation mask film; and a metallic mask film overlaying the barrier mask film. The method further includes the steps of etching a trench within the mask layer, through at least the metallic mask film, without

penetrating through the passivation layer and after etching the trench in the mask layer, then etching a via through the mask layer within the trench and through the low-k dielectric material to the underlying metal layer before transferring the trench to the low-k dielectric material.

In one embodiment of the invention, an interconnect layer 30 includes generally a via dielectric layer 31 over which is formed a trench dielectric layer 32. The layers 31 and 32 are separated by an etch stop layer 36. A mask layer 37, formed over the upper via dielectric layer 32, comprises three mask films: (1) a first film 38 being a passivation layer, e.g., silicon oxide or silicon carbide, formed on the dielectric layer 31; (2) a second mask film 39 comprising silicon nitride, deposited over the first film; and (3) a third mask film 40, formed over the second film, preferably comprises a refractory metal or a metal alloy. Provision of the metal in the third mask film 40 increases the etch selectivity, allowing for the effective and faithful transfer of a feature patterned 42 in the films 39 and 40 to the dielectric layers 31 and 32. (See, pages 6 – 8 and Figures 10-11).

Independent Claim 13 is directed to a method of forming an interconnect structure on an integrated circuit device having a low-k dielectric material deposited over an underlying metal layer and a mask layer deposited on a low-k dielectric material. The mask layer has a desired etch selectivity with respect to the low-k dielectric material. The method comprises the step of forming a non-metallic barrier layer interposed between a passivation layer and a metallic film to create a composite mask layer to increase the etch selectivity of the mask layer with respect to the low-k dielectric layer.

In one embodiment, an interconnect layer 30 includes generally a low-k dielectric layer 31 formed over a trench low-k dielectric layer 32, which are separated by an etch stop layer 36. A mask layer 37, formed over the upper via dielectric layer 32, comprises three mask films: (1) a first film 38

being a passivation layer, e.g., silicon oxide or silicon carbide, formed on the low-k dielectric layer 32; (2) a second non-metallic mask film 39, e.g. silicon nitride, deposited over the first film; and (3) a third metal mask film 40, e.g., titanium, tungsten, or tantalum, formed over the second film non-metallic mask film 39. Provision of the mask layer 37 increases the etch selectivity increase the etch selectivity of the mask layer with respect to the low-k dielectric layer film 32. (See, pages 6 – 8 and Figures 10-15).

Independent Claim 21 is directed to a method for the fabrication of a semiconductor device including a wafer substrate having a dielectric material that is formed over a metallization layer, which is formed over the wafer substrate. The method comprises forming a mask layer over the dielectric material wherein the mask layer includes a passivation film and has a known etch selectivity with respect to the dielectric material. A non-metallic barrier layer is formed over the passivation film and a metallic mask film is deposited over the barrier layer to increase the etch selectivity of the mask layer. A first feature is patterned in the mask layer after depositing the metallic mask film and etched through the metallic mask film without exposing the underlying dielectric material after patterning the feature in the mask layer. A second features is patterned in the mask layer and overlaps at least a portion of the first feature. The second feature is etched in the dielectric material in accordance with the patterned second feature in the mask layer before removing remaining portions of the passivation mask film and the metallic mask film. The first feature from the mask layer is transferred to the underlying dielectric material after etching the second feature through the dielectric material to the metallization layer, and a conductive metal is deposited in the first and second features.

In one embodiment, a mask layer 37 is formed over a dielectric material 31 and 32 wherein

the mask layer 37 includes a passivation film 38 (e.g., silicon or silicon carbide) and has a known etch selectivity with respect to the dielectric material 32. A non-metallic barrier layer 39, such as silicon nitride, is formed over the passivation film 38, and a metallic mask film 40, such as a refractory metal, is deposited over the non-metallic barrier layer 39 to increase the etch selectivity of the mask layer 37. A first feature 42 is patterned in the mask layer 37 after depositing the metallic mask film 40 and is etched through the metallic mask film 40 without exposing the underlying dielectric material 32 after patterning the feature in the mask layer 37. A second feature 44 is patterned in the mask 1ayer 37 and overlaps at least a portion of the first feature 42. The second feature 44 is etched in the dielectric material 31 and 32 in accordance with the patterned second 44 feature in the mask layer 37 before removing remaining portions of the passivation mask film 38 and the metallic mask film 40. The first feature 42 from the mask layer 37 is transferred to the underlying dielectric material 32 after etching the second feature 44 through the dielectric material 31 and 32 to the metallization layer 34, and a conductive metal 45 is deposited in the first and second features 42 and 44. (See, pages 6 – 10 and Figures 10-15).

Regarding dependent claims 7-10, the passivation layer 38 comprises silicon dioxide or silicon carbide, the barrier mask film 39 comprises silicon nitride, and the metallic mask film 40 comprises a refractory metal or a refractory metal alloy. (See, page 7, lines 14-31) In the more specific embodiment, of claim 10, the refractory metal is chosen from the group of refractory metals including titanium, tantalum and tungsten, and the refractory metal alloy is chosen from the group of refractory metal alloys comprising titanium nitride and tantalum nitride. (See, page 7, lines 26-31).

Regarding dependent claims 11 and 12, the method further includes the step of forming a photoresist layer 41 over the metallic mask film 37, (See, page 7, lines 14-21), patterning a trench

feature 42 in the photoresist layer 41, etching a trench 42 through the metal mask film 40 and the barrier mask film 39 to the passivation mask film 38. (See, page 8, lines 16-22).

Regarding dependent claims 14 and 15 of the method of claim 13, the metallic film 37 comprises a refractory metal or a refractory metal alloy wherein the refractory metal is chosen from the group of refractory metals including titanium, tantalum and tungsten and the refractory metal alloy is chosen from the group of refractory metal alloys including titanium nitride or tantalum nitride. (See, page 7, lines 26-31).

Regarding dependent claims 16, 17 and 18, the method of claim 13 further includes forming a passivation mask film 38 over the dielectric material 32, forming a barrier mask film 39 over the passivation mask film 38, and the metallic film 40 is formed over the barrier mask film 39. (See, page 7, lines 26-31). In the method of claim 15 the passivation mask film 38 comprises silicon dioxide or silicon carbide. (See, page 7, lines 14-21), and the barrier mask film 39 comprises silicon nitride. (See, page 7, lines 26-31).

Regarding claims 19 and 20, the method of claim 13 further includes etching a trench 42 within the low-k dielectric 32 material to a predetermined depth of the low-k dielectric material 32, etching a via 44 through the low-k dielectric material 32 and 31 to the underlying metal layer 34 of the low-k dielectric material 31, and depositing a conductive metal 45 within the via 44 and trench 42. (See pages 8-9). Regarding claim 20, the conductive metal 45 is deposited on the integrated circuit chip outside of the via 42 and the trench 44, and the method further includes the steps of planarizing the integrated circuit chip, and removing the excess conductive metal 45, the metallic mask layer 40 and the barrier mask film 39. (See, page 9, lines 14-31 and Figure 15).

Regarding claims 22-24, in the method of claim 21, the etching step comprises etching the

feature 42 in the mask layer 37 through the metallic mask film 40 and non-metallic barrier mask film 39 down to the passivation mask film 38, (See, page 8, lines 16-22), then removing the metallic mask film 40 and barrier mask film 39 after etching the first and second features 42, 44 in the dielectric material 32 and 31, and before depositing the conductive metal in the feature 45. (See, page 9, lines 14-22). In the method of claim 21, patterning includes patterning a first feature having a predetermined width different from a predetermined width of the first feature, and patterning a second feature having a predetermined width, the second feature being aligned with respect to the first feature. (See, page 8, lines 14-30, page 9, lines 1-7, and Figures 12-13). In the method claim 23, the etching step includes etching the first feature 42 in the mask layer 37 and through the metallic mask film 40 and to the passivation mask film 38 before patterning the second feature 44. Then the second feature 44 is etched. The second feature 44 is etched to a predetermined depth in the dielectric material 31, before etching the first feature 42 of the dielectric material 32 to a predetermined depth of the dielectric material 32 spaced above the predetermined depth of the second feature 44. (See, page 8, lines 14-30, page 9, lines 1-12, and Figures 12-14).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

All of the claims 6-24 have been finally rejected under 35 U.S.C. 103(a) as unpatentable over Chan, et al. (U.S. 6,312,874) in view of Usami (U.S. 6,468,898).

VII. APPELLANTS' ARGUMENT

The inventions set forth in independent Claims 6, 13, and 21 and their respective dependent claims are not obvious over the references on which the Examiner relies.

Rejection of Claims 6-24 under 35 U.S.C. 103(a) over Chan et al. (U.S. 6,312,874) in view of Usami (U.S. 6,468,898)

A. THE REJECTION REQUIRES AN IMPROPER RECONSTRUCTION OF THE PRIOR ART.

1. The rejection based on the combination of the Chan and Usami references requires a hindsight reconstruction of the claimed invention. This becomes most apparent when attempting to apply the references according to the Final Rejection. Any attempt to construct Appellants' invention from this prior art would require a piecemeal substitution of elements between the two references. The required substitutions are piecemeal and not taught or suggested by the prior art. In fact, the substitutions appear inconsistent with the teachings of the references. For specific reasons now presented, it must be concluded that these references fail to teach or suggest the claimed combinations.

B. NEITHER REFERENCE CONTAINS ANY TEACHING OR SUGGESTION FOR A MODIFICATION THAT MEETS THE CRITERIA NECESSARY TO SUSTAIN AN OBVIOUSNESS REJECTION.

The secondary reference, Usami, teaches two mask layer embodiments: (1) a combination of one SiO_2 and one metal layer (First Embodiment); and (2) a combination of one SiO_2 layer and two overlying metal layers (Second Embodiment). The primary reference, Chan, only teaches a three-layer embodiment wherein the lowest and uppermost layers are SiO_2 and a central layer is silicon nitride. The rejection combines a piece of the Second Embodiment of Usami into the three-layer embodiment of Chan to reconstruct the claimed invention. This would require undoing Chan's teaching that the lowest and uppermost layers are the same material, i.e., SiO_2 . This would also

require replacing one of the metal layers of the Usami combination with the silicon nitride central layer of Usami. The Usami reference only teaches a metallic central layer and there is no support for replacing this metallic central layer with a non-metallic, e.g., silicon nitride, central layer.

C. THE REJECTION IS IMPROPER BECAUSE THE PRIOR ART DOES NOT SUGGEST THE DESIRABILITY OF THE COMBINATION.

In sustaining the rejection, the Final Office Action states that it would have been obvious to so modify the Chan reference

> "in order to provide a good quality dual damascene structure using a multiple layer mask ...[and the] . . . combination is proper because both references are solving a common problem (Usami, col. 3, lines 64-67; Chan et al., Abstract, col. 3, lines 64-67) [See page 4 of Final office Action]."

The above statement only goes so far as to show that there is a general desire to overcome difficulties known to exist in the manufacture of dual damascene interconnects. This statement is not, by itself, a "suggestion to combine the references" as argued at page 4 of the Final Office Action.

The Final Office Action also concludes that both of the references are solving a common problem. Actually, each of the references addresses a different problem (e.g., protection of low-k dielectric material; and solving misalignment problems). Nowhere does the prior art suggest the desirability of the claimed combinations. MPEP 2143.01 makes clear that the mere fact references can be combined or modified in hindsight does not render the resulting combination obvious. (See again page 4 of the Final Office Action). The Examiner's combination was only made in view of Appellants' disclosure of a novel combination and there is no legitimate basis from which to argue otherwise.

Actually, the Examiner's above-citation of passages in Usami and Chan confirms that these references are not solving a common problem. The foregoing citations confirm that Chan addresses the problem of a misaligned via relative to a trench width, while Usami addresses preventing a low dielectric constant film from being subjected to a plasma ashing treatment. Even if the references were solving a common problem, this, alone, would not provide license to reconstruct the prior art references. The references cannot be combined piecemeal simply because there is a desire in the art to provide a better dual damascene structure. More is required. The references must contain a teaching or suggestion to make the combination. However, in this instance, the Chan reference contains teachings that are inconsistent with reconstructing the multiple layer 58 of Chan into Appellants' claimed "tri-layer." To sustain the rejection the prior art must suggest the desirability of the combination. See *In Re: Mills*, 916 F 2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)).

The Examiner cites *In re Keller*, 642 F. 2d 413, 208 USPQ 871 (CCPA 1981) for establishing the test for obviousness, and states "the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art (Final Office Application No. 101699,975 Action, page 61). However, the Examiner has not cited any teachings in either of the references to support the combination and, as noted above, reconstruction of Chan's multiple layer 58 is inconsistent with the express teachings of the Chan reference. In other words, the Chan reference teaches away from the Examiner's piecemeal reconstruction.

D. EACH OF THE CLAIMS IS PATENTABLY DISTINCT OVER THE PRIOR ART.

1. INDEPENDENT CLALM 6 IS PATENTPLBLY DISTINCT OVER ANY COMBINATION OF THE PRIOR ART.

Claim 6 requires, among other features, a tri-part mask layer including the combination of:

> **i. a passivation mask film over the low-k dielectric material; . .**
> **ii. a non-metallic barrier mask film overlaying the passivation mask film; and**
> **iii. a metallic mask film overlaying the barrier mask film ...**

The Final Rejection characterized the Chan reference as follows:

> "forming a tri-part mask layer (58) overlaying the low-K dielectric material . . . including a .. . film (52) [of] ... silicon oxide . . . on the low-K dielectric material (50), a non-metallic barrier mask film (54) made of silicon nitride . . . and third layer (56) overlaying . . . film (54) [see Final Office Action at page 2]."

In applying the Chan reference to the claims, the Examiner noted that this prior art "multiple layer mask (58)" protects the low-k dielectric material (50) (Final Office Action at page 2). However, as explained below, the Final Office Action also attempts, incorrectly, to characterize the Chan reference as being similar to both the claimed invention and the Usami teachings, stating that Chan:

> "teaches etching each mask layer **selectively without etching the rest of the layers** ..[see page 3 of Final Office Action Emphasis Added]"

In this regard, all embodiments of the invention covered by claim 6 differ from the Chan reference. The Chan reference specifically and only teaches a mask layer having a third (uppermost) layer 56 which is formed of insulator silicon dioxide. (See, Col. 5, line 14).

Chan only teaches a structure wherein both the lowest layer 52 and the uppermost layer 56 have been formed of silicon dioxide. Although the Chan reference discloses, at Col. 5, lines 10 – 17,

that the layers are "for example" silicon dioxide, the Chan reference discloses no other material compositions for either of these layers 52 and 56. Further, there is absolutely no suggestion that these layers 52 and 56 would be anything other than insulative layers, i.e., there is no support for replacing SiO_2 layers 52 and 56 with metal layers. To further illustrate this distinction between the claimed invention and the disclosure of Chan, note that the Chan reference expressly teaches the following relationship between the two silicon dioxide layers:

> "layer 56 [of silicon dioxide] . . . is made thicker than the . . . layer 52 [of silicon dioxide] ... For example, the . . . layer 52 may be 1000 A thick, and the . . . layer 56 may be 2000 A thick [Col5, lines 17-22]. "

The Chan reference also teaches using the same etchant, i.e., C_4F_8 for both of the layers 52 and 56. (See, Col. 6, line 57 and Col. 7, line 14). With the foregoing being the only disclosed examples relating to the layers 52 and 56, it is incorrect to conclude that the Chan reference teaches "etching each mask layer selectively without etching the rest of the layers." In fact, the process sequence shown in Figures 3c and 3d of the Chan reference illustrates how the layers 52 and 56 are not etched selectively. (See also, Col. 6, lines 5 -15 of the Chan reference). By all appearances, the layers are simultaneously etched at the same rate.

If, as suggested by the Examiner, one of the SiO_2 layers 52 or 56 of Chan were replaced with a metal layer, then the layers 52 and 56, as implied by the Examiner, would not have the same etch selectivities-although the Chan reference teaches or implies that the layers 52 and 56 do have the same selectivities. By all appearances, specifying the relative thicknesses of the layers 52 and 56 as taught by Chan assumes that the layers 52 and 56 are identical in order to have the same etch selectivity (also as taught by Chan.).

Notwithstanding the foregoing (but apparently embracing an incorrect conclusion-that Chan.

teaches that the layers 52 and 56 have different etch selectivities), the Final Rejection assumes it is appropriate to reconstruct the multiple layer 58 of Chan by replacing Chan's upper silicon dioxide layer 56 with a metal film, e.g., the tungsten film 37 described in the Usami reference (See, Col. 10, line 18). This is not consistent with the teaching in the Chan reference for the layers 52 and 56 to have the *same* selectivity.

The combination of Chan and Usarni also requires a reconstruction of Usami in order to meet the terms of the claimed invention. In this regard, the Usami reference discloses a first embodiment (Cols. 7-9) and a second embodiment (Cols. 9-12). In the first embodiment, a metal mask 15 (WN) is deposited over a SiO_2 film 4, i.e. a bi-layer comprising a metal film over an insulator film. (See, Figure 1A as well as Col. 7, lines 39–51). In the second embodiment (relied upon for the Examiner's combination) a tri-layer comprises (1) a first metal film 37 (W) formed over (2) a second metal film 35 (Ta) formed over (3) a SiO_2 film 24. (See Figure 4A as well as Col. 10, lines 14–23). In short, Usami teaches a first combination of one metal film and one film of SiO_2, and a second combination of two metal films and one film of SiO_2. Usami does not teach or suggest any combinations having one film of SiO_2, one non-metallic barrier film and one metal film.

Another reason it is improper to combine the references is that the Chan reference uses all three layers (SiO_2 layer 56, silicon nitride layer 54 and SiO_2 layer 52) to pattern and transfer the desired features to the low-k dielectric materials 46 and 50 (See, Chan at Col. 5, lines 53-55 and Col. 5, lines 58-61, and Col. 6, lines 5-21; see also Figs 3d-3h), while Usami (Second embodiment; (See, Col. 10, lines 26-32, Figs 4F, 5B and 5C)) uses the two uppermost (metal) layers 35 and 37-and not the lowermost (SiO_2) layer 24-to pattern and transfer the feature to the low-k (organic polymer) film 23. From the foregoing it becomes clear that the etch processes of the two references are different

and a substitution of a metal layer for the SiO_2 layer 56 of Chan is not consistent with using all three layers 56, 54 and 52 to pattern and transfer the features, since the etch process of Chan. requires the same etch selectivity of the SiO_2 layers 52 and 56.

With regard to claim 6, it is only the Appellants who teach or suggest formation of a tri-part mask layer (overlaying a low-k dielectric material) which includes:

> i. a passivation mask film over the low-k dielectric material; . .
> ii. a non-metallic barrier mask film overlaying the passivation mask film; and
> iii. a metallic mask film overlaying the barrier mask film;

For the above reasons, none of the references, alone or in combination, can be shown to teach or suggest this combination. Furthermore, claim 6 is allowable over the combination for additional reasons as described below with reference to claim 13.

2. INDEPENDENT CLAIM 13 IS PATENTABLY DISTINCT OVER ANY COMBINATION OF THE PRIOR ART.

The method of Claim 13 requires, for a mask layer deposited on low-k dielectric material the feature of:

> "forming a non-metallic barrier layer interposed between a passivation layer and a metallic film to create a composite mask layer to increase the etch selectivity of the mask layer with respect to the low-k dielectric layer."

The Final Rejection characterized the prior art as follows:

> "Chan et al. does not specifically show forming a metallic mask film over the barrier mask film. However, Usami discloses forming a silicon dioxide film (or silicon carbide) (24) over the low-K dielectric material, forming a mask (35) (barrier mask film), forming a metallic mask film (37) over the mask (35) (Fig. 4A, Col. 9, lines 62-67, Col. 10, lines 5-22)."

The cited passage (Col. 10, lines 5-22) reveals that the above characterization of the Usami

reference, e.g., Fig. 4A, is incorrect. Usami does not disclose the film 35 to be a barrier mask film. Rather, Usami teaches that the "Ta (tantalum) film 35 . . . serves as a first metal mask . . ." (See, Col. 10, lines 16–18).

If the layer 35 of Usami were a non-metallic barrier layer, then it might be argued that the references could be combined by merely substituting the SiO_2 layer 56 (in the Chan reference) with the layer 35 of Usami. However, even then the combination would be impermissible for at least the following two reasons, as more fully presented above with regard to claim 6.

The combination is inconsistent with the teaching in the Chan reference for the layers 52 and 56 to have the *same* selectivity. The etch processes of the two references are so different that a substitution of a metal layer for the SiO_2 layer 56 of Chan is not consistent with the teachings of Chan. In the etch process of Chan, all three layers 52, 54 and 56 are used to transfer the desired pattern. Accordingly, Chan teaches that the SiO_2 layers 52 and 56 have the same etch selectivity. In contrast, Usami only uses the two uppermost (metal) layers 35 and 37-and not the lowermost (SiO_2) layer 24 to pattern and transfer the feature to the low-k (organic polymer) film 23. If the SiO_2 layer of Chan is replaced with the metal layer of Usami, the layers 52 and 56 will not have the same selectivity.

For the above reasons, none of the references, alone or in combination, can be shown to teach or suggest the above-quoted features of claim 13. Furthermore, claim 13 is allowable over the combination for additional reasons as already described with reference to claim 6.

3. INDEPENDENT CLAIM 21 IS PATENTABLY DISTINCT OVER ANY COMBINATION OF THE PRIOR ART.

The method of Claim 21 requires, for the fabrication of a semiconductor device:

(a) forming a mask layer over the dielectric material wherein said mask layer includes a passivation film . . .

(b) forming a non-metallic barrier layer over the passivation film;

(c) depositing a metallic mask film over the barrier layer to increase the etch selectivity of the mask layer;

(d) patterning a first feature in the mask layer after depositing the metallic mask film . . .

Chan teaches away from the invention of claim 21. Instead of "depositing a metallic mask film over the barrier layer to increase the etch selectivity" the Chan reference teaches selection of SiO_2 for the layer 56.

Notwithstanding this inconsistency between the claimed invention and the primary reference, the rejection transgresses the teaching in the Chan reference to provide the same material for the layer 56 as the layer 52. The Chan reference teaches provision of the same selectivity for layers 52 and 56 while making the layer 56 relatively thick compared to the layer 52, thereby providing layers 52 and 56 with the same selectivity. Also, as noted above with regard to claim 6, the Chan reference uses three layers 52, 54 and 56 to pattern and transfer features to the underlying dielectric, while the Usami reference only discloses use of the two uppermost (metal) layers 35 and 37-and not the lowermost (SiO_2) layer 24 to pattern and transfer features to the low-k (organic polymer) film 23. If the SiO_2 layer of Chan is replaced with the metal layer of Usami, then the layers 52 and 56 will not have the same selectivity as required by Chan in order to transfer the features to the underlying dielectric.

For all of these reasons, none of the references, alone or in combination, can be shown to

teach or suggest the above-quoted features of claim 21. Furthermore, claim 21 is allowable over the combination for additional reasons as already described with reference to claims 6 and 13.

4. CLAIM 7 IS PATENTABLY DISTINCT OVER ANY COMBINATION OF THE PRIOR ART.

Claim 7 depends directly from claim 6 and includes as part of the combination of features that said passivation mask film comprises silicon dioxide or silicon carbide. None of the art of record, alone or in combination, teaches or suggests the combination of features covered by claim 7. Moreover, although the Final Office Action states otherwise, the Usami reference (See, Col. 10, lines 5-22) does not suggest use of silicon carbide.

5. CLAIM 8 IS PATENTABLY DISTINCT OVER ANY COMBINATION OF THE PRIOR ART.

Claim 8 depends directly from claim 6 and includes as part of the combination of features that "said barrier mask film comprises silicon nitride." None of the art of record, alone or in combination, teaches or suggests the combination of features covered by claim 8.

6. CLAIM 9 IS PATENTABLY DISTINCT OVER ANY COMBINATION OF THE PRIOR ART.

Claim 9 depends directly from claim 6 and includes as part of the combination of features that "said metallic mask film comprises a refractory metal or a refractory metal alloy." None of the art of record, alone or in combination, teaches or suggests the combination of features covered by claim 9.

7. CLAIM 10 IS PATENTABLY DISTINCT OVER ANY COMBINATION OF THE PRIOR ART.

Claim 10 depends directly from claim 9 and includes as part of the combination of features that "said refractory metal is chosen from the group of refractory metals including titanium, tantalum and tungsten, and said refractory metal alloy is chosen from the group of refractory metal alloys comprising titanium nitride and tantalum nitride." None of the art of record, alone or in combination, teaches or suggests the combination of features covered by claim 9.

8. CLAIM 11 IS PATENTABLY DISTINCT OVER ANY COMBINATION OF THE PRIOR ART.

Claim 11 depends directly from claim 6 and includes as part of the combination of features "the step of forming a photoresist layer over the metallic mask film, patterning a trench feature in the photoresist layer, etching a trench through the metal mask film and the barrier mask film to the passivation mask film." None of the art of record, alone or in combination, teaches or suggests the combination of features covered by claim 9.

9. CLAIM 12 IS PATENTABLY DISTINCT OVER ANY COMBINATION OF THE PRIOR ART.

Claim 12 depends directly from claim 11 and includes as part of the combination of features "the step of forming a photoresist layer over the low-k dielectric material, and patterning a via feature in the photoresist layer." None of the art of record, alone or in combination, teaches or suggests the

combination of features covered by claim 9.

10. CLAIM 14 IS PATENTABLY DISTINCT OVER ANY COMBINATION OF THE PRIOR ART.

Claim 14 depends directly from claim 13 and includes as part of the combination of features that the "metallic film comprises a refractory metal or a refractory metal alloy." None of the art of record, alone or in combination, teaches or suggests the combination of features covered by claim 14.

11. CLAIM 15 IS PATENTABLY DISTINCT OVER ANY COMBINATION OF THE PRIOR ART.

Claim 15 depends directly from claim 14 and includes as part of the combination of features that "said refractory metal is chosen from the group of refractory metals including titanium, tantalum and tungsten, and said refractory metal alloy is chosen from the group of refractory metal alloys comprising titanium nitride or tantalum nitride, and the metallic film comprises a refractory metal or a refractory metal alloy." None of the art of record, alone or in combination, teaches or suggests the combination of features covered by claim 14.

12. CLAIM 16 IS PATENTABLY DISTINCT OVER ANY COMBINATION OF THE PRIOR ART.

Claim 16 depends directly from claim 13 and includes as part of the combination of features "forming a passivation mask film over the dielectric material, forming a barrier mask film over the passivation mask film and said metallic film is formed over the barrier mask film." None of the art

of record, alone or in combination, teaches or suggests the combination of features covered by claim 16.

13. CLAIM 17 IS PATENTABLY DISTINCT OVER ANY COMBINATION OF THE PRIOR ART.

Claim 17 depends directly from claim 15 and includes as part of the combination of features that "said passivation mask film comprises silicon dioxide or silicon carbide." None of the art of record, alone or in combination, teaches or suggests the combination of features covered by claim 17.

14. CLAIM 18 IS PATENTABLY DISTINCT OVER ANY COMBINATION OF THE PRIOR ART.

Claim 18 depends directly from claim 15 and includes as part of the combination of features that "said barrier mask film comprises silicon nitride." None of the art of record, alone or in combination, teaches or suggests the combination of features covered by claim 16.

15. CLAIM 19 IS PATENTABLY DISTINCT OVER ANY COMBINATION OF THE PRIOR ART.

Claim 19 depends directly from claim 13 and includes as part of the combination of features "the steps of etching a trench within the low-k dielectric material .to a predetermined depth of the low-k dielectric material, etching a via through the low-k dielectric material to the underlying metal layer of the low-k dielectric material, and depositing a conductive metal within the via and trench." None of the art of record, alone or in combination, teaches or suggests the combination of features

covered by claim 19.

16. CLAIM 20 IS PATENTABLY DISTINCT OVER ANY COMBINATION OF THE PRIOR ART.

Claim 20 depends directly from claim 19 and includes as part of the combination of features that "the conductive metal is deposited on the integrated circuit chip outside of the via and the trench and the method further including the steps of planarizing the integrated circuit chip, and removing said excess conductive metal, the metallic mask layer and the barrier mask film." None of the art of record, alone or in combination, teaches or suggests the combination of features covered by claim 20.

17. CLAIM 22 IS PATENTABLY DISTINCT OVER ANY COMBINATION OF THE PRIOR ART.

Claim 22 depends directly from claim 21 and includes as part of the combination of features that "said etching step comprises the step of etching the feature in the mask layer through the metallic mask film and non-metallic barrier mask film down to the passivation mask film, then removing the metallic mask film and barrier mask film after etching the first and second features in the dielectric material, and before depositing the conductive metal in the feature." None of the art of record, alone or in combination, teaches or suggests the combination of features covered by claim 16.

18. CLAIM 23 IS PATENTABLY DISTINCT OVER ANY COMBINATION OF THE PRIOR ART.

Claim 23 depends directly from claim 21 and includes as part of the combination of features

that "said step of patterning includes patterning a first feature having a predetermined width different from a predetermined width of the first feature, and patterning a second feature having a predetermined width, said second feature being aligned with respect to said first feature." None of the art of record, alone or in combination, teaches or suggests the combination of features covered by claim 16.

19. CLAIM 24 IS PATENTABLY DISTINCT OVER ANY COMBINATION OF THE PRIOR ART.

Claim 24 depends directly from claim 23 and includes as part of the combination of features that "said etching step includes etching the first feature in the mask layer through the metallic mask film and to the passivation mask film before patterning the second feature, and then etching the second feature a predetermined depth in the dielectric material, before etching the first feature of the dielectric material to a predetermined depth of the dielectric material spaced above the predetermined depth of the second feature." None of the art of record, alone or in combination, teaches or suggests the combination of features covered by claim 16.

E. THE BASIS FOR REJECTION OF CLAIMS 6-24 UNDER 35 U.S.C. §103(a) IS NOT SUPPORTED BY THE CITED ART.

There is no suggestion or motivation to combine the disclosures of Chan and Usami, or to perform a piecemeal reconstruction of the prior art as required to meet the terms of Appellants' claims. Nor is such a suggestion or motivation present in the ordinary knowledge of one skilled in the art. The Final Office Action states that "the suggestion to combine the references is to provide a

good quality dual damascene structure . . . "

As has been explained herein, each of the references teaches away from a combination, as well as a piecemeal reconstruction. An invention will not be rendered obvious merely by combining teachings found in the prior art. There must be some suggestion or incentive in the prior art to make the combination. The prior art must suggest that the combination would have a reasonable likelihood of success. *In re Bolduc*, 1992 U.S. App. LEXIS 2480 (Fed. Cir., 1992). The Appellants are aware of no prior art that suggests a reasonable likelihood of success associated with the combination of the Chan and Usami references.

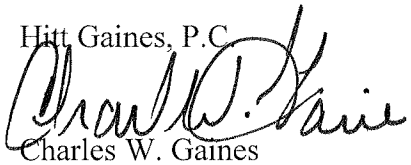
Thus, the rejection of the claims 6-24 under Section 103(a) is not supported by the cited art and should be withdrawn since the combination of the prior art patents to Chan and Usami do not render obvious any of the claims.

VIII. APPENDICES

An appendix containing a copy of the claims (6-24) involved in this appeal is provided herewith. No other appendix is provided.

Respectfully submitted,

Hitt Gaines, P.C.



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VIII. APPENDIX A-CLAIMS

6. A method of forming a dual damascene interconnect structure of an integrated circuit device, said interconnect structure having a low-k dielectric material deposited over an underlying metal layer, comprising the steps of:

a. forming a tri-part mask layer overlaying the low-k dielectric material, the mask layer including:

i. a passivation mask film over the low-k dielectric material;

ii. a non-metallic barrier mask film overlaying the passivation mask film; and

iii. a metallic mask film overlaying the barrier mask film;

b. etching a trench within the mask layer, through at least the metallic mask film, without penetrating through the passivation layer ; and

c. after etching the trench in the mask layer, then etching a via through the mask layer within the trench and through the low-k dielectric material to the underlying metal layer before transferring the trench to the low-k dielectric material.

7. The method of claim 6 wherein said passivation mask film comprises silicon dioxide or silicon carbide.

8. The method of claim 6 wherein said barrier mask film comprises silicon nitride.

9. The method of claim 6 wherein said metallic mask film comprises a refractory metal or a refractory metal alloy.

10. The method of claim 9 wherein said refractory metal is chosen from the group of refractory metals including titanium, tantalum and tungsten, and said refractory metal alloy is chosen from the group of refractory metal alloys comprising titanium nitride and tantalum nitride.

11. The method of claim 6 further including the step of forming a photoresist layer over the metallic mask film, patterning a trench feature in the photoresist layer, etching a trench through the metal mask film and the barrier mask film to the passivation mask film.

12. The method of claim 11 further including the step of forming a photoresist layer over the low-k dielectric material, and patterning a via feature in the photoresist layer.

13. The method of forming an interconnect structure on an integrated circuit device having a low-k dielectric material deposited over an underlying metal layer, and a mask layer deposited on the low-k dielectric material, and said mask layer having a desired etch selectivity with respect to the low-k dielectric material, the method comprising the step of forming a non-metallic barrier layer interposed between a passivation layer and-a metallic film to create a composite mask layer to increase the etch selectivity of the mask layer with respect to the low-k dielectric layer

14. The method of claim 13 wherein said metallic film comprises a refractory metal or a refractory metal alloy.

15. The method of claim 14 wherein said refractory metal is chosen from the group of refractory metals including titanium, tantalum and tungsten and said refractory metal alloy is chosen from the group of refractory metal alloys including titanium nitride or tantalum nitride.

16. The method of claim 13 further including the steps of forming a passivation mask film over the dielectric material, forming a barrier mask film over the passivation mask film and said metallic film is formed over the barrier mask film.

17. The method of claim 15 wherein said passivation mask film comprises silicon dioxide or silicon carbonite.

18. The method of claim 15 wherein said barrier mask film comprises silicon nitride.

19. The method of claim 13 further including the steps of etching a trench within the low-k dielectric material to a predetermined depth of the low-k dielectric material, etching a via through the low-k dielectric material to the underlying metal layer of the low-k dielectric material, and depositing a conductive metal within the via and trench.

20. The method of claim 19 wherein the conductive metal is deposited on the integrated circuit chip outside of the via and the trench and the method further including the steps of planarizing the integrated circuit chip, and removing said excess conductive metal, the metallic mask layer and the barrier mask film.

21. A method for the fabrication of a semiconductor device including a wafer substrate having a dielectric material formed over a metallization layer formed over said wafer substrate, comprising the steps of:

(a) forming a mask layer over the dielectric material wherein said mask layer includes a passivation film, and said mask layer having a known etch selectivity with respect to the dielectric material;

(b) forming a non-metallic barrier layer over the passivation film;

(c) depositing a metallic mask film over the barrier layer to increase the etch selectivity of the mask layer;

(d) patterning a first feature in the mask layer after depositing the metallic mask film;

(e) etching the first feature through the metallic mask film without exposing the underlying dielectric material after patterning the feature in the mask layer; (f) patterning a second feature in the mask 1ayer;said second feature overlapping at least a portion of the first feature;

(g) etching the second feature in the dielectric material in accordance with the patterned second feature in the mask layer before removing remaining portions of the passivation mask film and the metallic mask film;

(h) transferring the first feature from the mask layer to the underlying dielectric material after etching the second feature through the dielectric material to the metallization layer; and

(i) depositing a conductive metal in the first feature and in the second feature.

22. The method of claim 21 wherein said etching step comprises the step of etching the feature in the mask layer through the metallic mask film and non-metallic barrier mask film down to the

passivation mask film, then removing the metallic mask film and barrier mask film after etching the first and second features in the dielectric material, and before depositing the conductive metal in the feature.

23. The method of claim 21 wherein said step of patterning includes patterning a first feature having a predetermined width different from a predetermined width of the first feature, and patterning a second feature having a predetermined width, said second feature being aligned with respect to said first feature.

24. The method of claim 23 wherein said etching step includes etching the first feature in the mask layer through the metallic mask film and too the passivation mask film before patterning the second feature, and then etching the second feature, and then etching the second feature a predetermined depth in the dielectric material, before etching the first feature of the dielectric material to a predetermined depth of the dielectric material spaced above the predetermined depth of the second feature.

IX. APPENDIX B-EVIDENCE

The evidence in this appendix includes U.S. Patent to Chan et al. (U.S. 6,312,874) and U.S. Patent to Usami (U.S. 6,468,898), which were entered in the record by the Examiner with the first Examiner's Office Action mailed April 15, 2005.